

Glossary of Advanced Packaging:

ACA	Anisotropic Conductive Adhesive Adhesive with conducting filler particles where the electrical conductivity is achieved only in z-direction under mechanical pressure.
Bare Die	Non-encapsulated silicon chip in singulated form
BCB	Benzocyclobutene Polymer dielectric from Dow Chemical used for wafer-level redistribution.
BGA	Ball Grid Array IC single or multichip package with an area of solder balls attached on the bottom side of a package.
BLT	Bondline Thickness The thickness of adhesive between two adherands.
BT	Bismaleimide Triazine High temperature organic substrate material mainly used for overmolded ball grid arrays (BGA).
C4	Controlled Collapse Chip Connection The classical flip chip technique from IBM using evaporated Pb-base solder.
CBGA	Ceramic Ball Grid Array Ball grid array using a ceramic carrier/wiring board.
CCC	Ceramic Chip Carrier Chip carrier with ceramic wiring board.
CCGA	Ceramic Column Grid Array Area array component with ceramic wiring board using solder columns of high lead solder alloy instead of eutectic solder balls.
CDIP or CerDIP	Ceramic Dual In-line Package Through-hole mount package (Pin-Through-Hole = PTH) made in cofired ceramic with two rows of pins on the opposite long sides of the package.
CLCC	Ceramic Leaded Chip Carrier Surface mount technology (SMT) package made in cofired ceramic with leads e.g. J-formed leads.
COB	Chip On Board Assembly of one or more bare dice on a substrate with electrical interconnection by wire bonding.
COF	Chip On Flex Special case of chip on board (COB) where the substrate is flexible e.g. polyimide.
CPGA	Ceramic Pin Grid Array Through-hole mount package (Pin-Through-Hole = PTH) made in cofired ceramic with an area array of pins.

CQFP	Ceramic Quad Flat Package Surface mount technology (SMT) package made in cofired ceramic with leads e.g. J-formed or gull-wing leads.
CSP	Chip Size Package or Chip Scale Package After packaging the component size is roughly the die size.
DCA	Direct Chip Attach Mounting bare dice directly on the wiring board in chip on board (COB) or flip chip on board technology.
Die	A small piece of silicon wafer, bounded by adjacent scribe lines in horizontal and vertical directions, that contains the complete device being manufactured. Also called chip and microchip and plural is called "dice."
Die Attach	The process of attaching the die to the substrate or leadframe by using a specified type of epoxy adhesive (or solder, glass frit, or using eutectic bonding).
Dicing	The separation of a semiconductor wafer into individual dice normally performed by a saw with a rotating blade with embedded diamond particles.
Die Bonding	The attachment of an integrated circuit chip to a substrate or header.
DIP	Dual In-line Package is the traditional buglike packages that have anywhere from 8 to 40 legs, evenly divided on two opposite sides of the package.
Epoxy Seal	A method of nonhermetically sealing a lid to a package.
ESD	Electro-Static Discharge Special measures are necessary to prevent a CMOS integrated circuit from damage by electrostatic discharge.
FBGA	Fine-Pitch Ball Grid Array Ball grid array with a fine pitch of ≤ 0.5 mm.
FC	Flip Chip Assembly of a bare die upside down directly on the substrate with simultaneous interconnection via bumps.
FCBGA	Flip Chip BGA Ball grid array type carrier using flip chip in package.
FCIP	Flip Chip In Package Flip chip technology used on a module carrier, e.g. on a ball grid array (BGA) or chip scale package (CSP) substrate, or in a molded leadframe package (instead of flip chip assembly on the main board).
FCOB	Flip Chip On Board Flip chip assembly on the main system board.
Flux	A material used to promote fusion or joining of metals in soldering and brazing. In soldering, a material that breaks down surface oxides.
FR4	Standard printed circuit board (PCB) material. (Flame Retardant composition 4)

Frit Seal	A method of hermetically sealing a ceramic lid by glass frit.
HASL	Hot Air Solder Leveling Standard surface finish (solder on copper) of printed circuit boards (PCB) for surface mount technology (SMT).
HAST	Highly Accelerated Stress Test Stress test by accelerated aging, e.g. in damp heat atmosphere, for reliability analysis.
HDI	High Density Interconnect Printed circuit board (PCB) substrate in fine-line multilayer technology e.g. build-up technology with micro vias.
HTCC	High Temperature Cofired Ceramic Multilayer ceramic substrate or package made by simultaneous sintering of alumina ceramic and tungsten metallization at a firing temperature of approx. 1500°C.
IC	Integrated Circuit
ICA	Isotropic Conductive Adhesive Adhesive with conducting filler particles e.g. Ag-epoxy leading to isotropic electrical conductivity due to the contact of conducting particles.
KGD	Known Good Die A tested bare chip that has the same level of performance, reliability, and quality as its packaged version. Typically used in multichip modules.
LCC	Leaded Chip Carrier Chip carrier for surface mount technology with leads e.g. J-formed leads.
LLCC	Leadless Chip Carrier Chip carrier for surface mount technology with side contacts running into lands at the bottom of the package.
LCCC	Leadless Ceramic Chip Carrier Ceramic chip carrier for surface mount technology with side contacts running into lands at the bottom of the package.
LTCC	Low Temperature Cofired Ceramic Multilayer ceramic substrate or package made by simultaneous sintering of alumina glass ceramic and copper or silver metallization at a firing temperature < 900°C.
µBGA	Micro Ball Grid Array Chip scale package (CSP) developed by Tessera Corp.
MCM	Multi-Chip Module Assembly of two or more bare dice on a substrate by any bonding technology.
MCM-C	MCM on a Ceramic substrate Multichip module using high temperature cofired ceramic (HTCC), low temperature cofired ceramic (LTCC) or multilayer thickfilm substrate technology.
MCM-D	MCM on a Deposited (metal/ dielectric) substrate Multichip module using layer deposition technology, e.g. physical vapour deposition (PVD), on ceramic or silicon substrates.

MCM-L	MCM on a L aminate substrate Multichip module using printed circuit board (PCB) technology, often fine-line multilayer technology (high density interconnect, sequential build-up)
MCP	Multi-Chip Package Through-hole or surface mount package containing two or more dice.
PBGA	Plastic B all G rid A rray Ball grid array with a printed circuit board (PCB) substrate and polymer encapsulation, e.g. by glob top or overmold.
PCB	Printed Circuit B oard A printed wiring board on which chips and other components are placed.
PDIP	Plastic D ual I n-line P ackage Through-hole mount package (Pin-Through-Hole = PTH) made in molded leadframe technology with two rows of pins on the opposite long sides of the package.
PGA	Pin G rid A rray IC package with an area array of pins attached to the bottom side of the package.
Pitch	The distance between the centers of adjustment pins, pads, bumps and solder balls.
PLCC	Plastic L eaded C hip C arrier Surface mount technology (SMT) package made in molding or overmolding technology with leads e.g. J-formed leads.
PPGA	Plastic P in G rid A rray IC package with printed circuit board (PCB) carrier and polymer encapsulation with an area array of pins.
PQFP	Plastic Q uad F lat P ackage Standard surface mount technology (SMT) package.
PTH	Pin-Through-Hole or Plated-Through-Hole A method of obtaining electrical connection between components and substrate by soldering component leads (or pins) inserted in plated through-holes.
PWB	Printed W iring B oard. A substrate of epoxy glass or other (basically organic) material on which a pattern of conductive traces is formed to interconnect the components that will be mounted upon it.
QFP	Quad F lat P ackage Standard surface mount technology (SMT) package.
SBB	Solderball B umper Automate equipment for sequential application of solder balls which are attached by laser soldering. or Stud Bump B onding Flip chip process using isotropic conductive adhesive (ICA) dip transfer in combination with Au stud bumps.

SCM	Single Chip Module or single chip package, module or package containing only one die.
SGA	Solder Grid Array Area array package with solder balls or columns.
SIP	Single In-Line Package Through-hole mount package (Pin-Through-Hole = PTH) with a single row of pins. or System In Package A single component, multi-function, multi-chip package providing all the needed system-level functions. Functions include analog, digital, optical, RF and MEMS (multichip module which is a subsystem in a package).
SMD	Surface Mount Device Standard component for surface mount technology (SMT).
SMT	Surface Mount Technology Technology where packaged components are mounted and soldered on top of a printed wiring board (no pin-through hole).
SO	Small Outline Standard surface mount technology (SMT) package.
SOC	System On a Chip A highly integrated device composed of multiple functional blocks, including on-chip memory and a processor (complete system in one IC).
SOIC	Small Outline Integrated Circuit Standard surface mount technology (SMT) package.
SOJ	Small-Outline Package, J-leaded Standard surface mount technology (SMT) package.
SOP	Small Outline Package Standard surface mount technology (SMT) package.
Substrate	A material which serves as the base for the mechanical and electrical connections of ICs (wiring board).
TAB	Tape Automated Bonding Chip interconnection technology similar to flip chip using a flex tape.
Thermosonic bonding	The bonding of wires to metal pads on an integrated circuit (and substrate resp. leadframe) by means of heat and ultrasonic scrubbing of the wire on the pad to create a metallurgical bond.
THT	Through-Hole Technology Technology for mounting packaged components on a printed wiring board where the components have pins which are inserted and soldered in plated holes of the board.
TQFP	Thin Quad Flat Package Standard surface mount technology (SMT) package, low profile.
TSOP	Thin Small-Outline Package Standard surface mount technology (SMT) package, low profile.

UBM	Under Bump Metallurgy or Under Bump Metallization Additional metallization applied on the pads of the wafer prior to the bumping.
Underfill	Encapsulant material typically deposited between a flip chip device and substrate used to reduce the mechanical stress resulting from a mismatch in the coefficient of thermal expansion (CTE) between the device and the substrate.
Ultrasonic bonding	The bonding of wires to metal pads on an integrated circuit (and substrate resp. leadframe) by means of a pressing mechanism at ambient temperature ultrasonically vibrating at a higher frequency of >10 kHz.
Wafer bumping	Process of applying bumps to the wafer (or die) pads so they can be utilised for flip chip or tape automated bonding (TAB) interconnection.
WB	Wire Bonding Technology for electrically connecting a die to a leadframe or substrate by bonding thin Au or Al wires with a typical wire thickness of 25 µm.
WL-CSP	Wafer-Level Chip Size Package Chip size package which is totally manufactured on wafer level.
Wire Bonding	The primary method of electrically connecting a die to a package via wire loops.
WLP	Wafer Level Packaging Additional wafer processing step to produce a chip size package (CSP), e.g. by redistribution technology and solder balling.

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